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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,078	08/27/2003	Frederick A. Perner	200205668-1	4664

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EXAMINER	
LE, THONG QUOC	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 03/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/649,078	PERNER ET AL.	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-28 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-28 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 23 August 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Pre-amendment filed on August 23, 2004 has been entered.

2. Claims 1-28 are presented for examination.

Information Disclosure Statement

3. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 02/03/2005.

4. Information disclosed and list on PTO 1449 was considered.

Drawings

5. The drawings were received on 08/23/2004. These drawings are acceptable.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 6-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Nishimura et al. (U.S. Patent No. 6,713,830).

Regarding claim 6-13, Nishimura et al. disclose a memory device (Figure 33) comprising a plurality of memory magnetic memory element (101,102..Column 18, lines 17-18),

a write circuit (219,220..) including a plurality of transistors that are coupled to a memory write line (312-324) ; wherein individual transistors within the plurality of transistors are in parallel (Figure 33) and have their conduction states modified independent of each other; and whereby the amount of voltage available to the magnetic memory element is increased (Column 17, lines 58-67,Column 19, lines 20-47), and further comprising logic coupled to the plurality of transistors, wherein the logic modifies the conduction state of individual transistors (223), and wherein the individual transistors within the plurality of transistors are binary weighted (Figure 33), and further comprising a first and second plurality of transistors, wherein the first plurality of transistors source current in the memory write lines and the second plurality of transistors sink current from the memory write lines, and wherein the first plurality of transistors comprise p-channel metal oxide semiconductor field effect transistors ("MOSFETs"), and the second plurality of transistors comprise n-channel MOSFETS (Figure 33), and wherein the logic is coupled to the gate terminals of the plurality of transistors (Figure 33), and wherein the amount of current in the write line controlled by

modifying the conduction state of individual transistors within the plurality of transistors, and a power supply coupled to the write circuit, wherein the power supply has approximately constant voltage and provides a variable current (Column 17, lines 44-67).

8. Claims 14-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Hidaka (Pub. U.S. Patent No. 2004/0095804).

Regarding claims 14-19, Hidaka discloses a memory (Figure 1), comprising: at least one memory write line (ABSTRACT) that is magnetically coupled to at least one magnetic memory element (MC), a write circuit including first and second transistors that are coupled to either end of the memory write line (Figure 1, 50) ; wherein the conduction state of the first transistor is controlled by an inverter circuit (Figure 1, 52,54), wherein the inverter circuit electrically couples a write signal to the first transistor (WT), and whereby the amount of voltage provided to the magnetic memory element is increased [0019, 0038], and wherein the conduction state of the first transistor is varied as the write signal is varied, and wherein a control signal is coupled to the input of the inverter and controls the conduction state of the inverter(Figure 1), and wherein the threshold voltage for the inverter is varied as the write signal is varied [0043], and a power supply coupled to the write circuit, wherein the power supply has approximately constant voltage and provides a variable current (Figure 1), and wherein the first transistor sources current to the memory write line and the second transistor sinks current from the memory write line (Figure 1).

Regarding claims 20-28, Hidaka discloses a circuit for controlling current (Figure 1, 5) to a magnetic memory array, comprising providing means for providing current to a conductor [0069], sinking means for sinking current from the conductor [0070-0075], wherein said conductor is magnetically coupled to coupled to a magnetic memory element [Figure 1], and a controlling means for controlling the conduction state of said providing means and said sinking means, and wherein altering said conduction state results in altering the digital state of the magnetic memory element, and means for supplying power to the circuit, and wherein the means for supplying power has approximately constant voltage and provides a variable current (Figure 1), and a processor (Figure 1, 5).

Regarding claims 1-5, the apparatuses discussed above would perform the claimed method 1-5.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827

THONG LE
PRIMARY EXAMINER